IN THE SPECIFICATION

At page 3, line 27, please add the following:

REFERENCES

B. Dipert et al., "Flash Memory Goes Mainstream," IEEE Spectrum, pp. 48-52 (Oct. 1993);

S.M. Sze, "Physics of Semiconductor Devices," John Wiley & Sons, New York (1969), p. 496;

S.R. Pollack et al., "Electron Transport Through Insulating Thin Films," Applied Solid State Science, Vol. 1, Academic Press, New York, (1969), p. 354;

D.A. Baglee, "Characteristics and Reliability of 100 Å Oxides," Proc. 22nd Reliability Symposium, (1984), p. 152;

V. M. Bermudez et al. "The Growth and Properties of Al and AlN films on GaN" J. Appl. Physics, Vol. 79, No. 1, pp. 110-119 (1996);

I. Akasaki et al. "Effects of AlN Buffer Layer on Crystallographic Structure and On Electrical and Optical Properties of GaN and $Ga_{1-x}Al_xN$ Films Grown on Sapphire Substrate by MOVPE," J. Of Crystal Growth, Vol. 98, pp. 209-19, North Holland, Amsterdam (1989);

The paragraph beginning at page 8, line 5 is amended as follows:

The present invention discloses a memory cell such as, for example, a dynamic electrically alterable programmable read only memory (DEAPROM) cell. The memory cell has a floating electrode, which is defined as an electrode that is "electrically isolated" from conductors and semiconductors by an insulator such that charge storage upon and removal from the floating electrode depends upon charge conduction through the insulator. In one embodiment, described below, the floating electrode is a floating gate electrode in a floating gate field-effect transistor, such as used in flash electrically erasable and programmable read only memories (EEPROMs). However, a capacitor or any other structure having a floating electrode and adjacent insulator could also be used according to the techniques of the present invention described below. According to one aspect of the present invention, a barrier energy between the floating electrode and the insulator is lower than the barrier energy between polycrystalline silicon (polysilicon) and silicon dioxide (SiO_2), which is approximately 3.3 eV. According to another aspect of the present invention, the shorter retention time of data charges on the floating

electrode, resulting from the smaller barrier energy, is accommodated by refreshing the data charges on the floating electrode. In this respect, the memory operates similar to a memory cell in a dynamic random access memory (DRAM). These and other aspects of the present invention are described in more detail below.

The paragraph beginning at page 8, line 23 is amended as follows:

Figure **1** is a simplified schematic/block diagram illustrating generally one embodiment of a memory **100** according to one aspect of the present invention, in which reduced barrier energy floating electrode memory cells are incorporated. Memory **100** is referred to as a dynamic electrically alterable programmable read only memory (DEAPROM) in this application, but it is understood that memory **100** possesses certain characteristics that are similar to DRAMs and flash EEPROMs, as explained below. ~~For a general description of how a flash EEPROM operates, see B. Dipert et al., "Flash Memory Goes Mainstream," IEEE Spectrum, pp. 48-52 (Oct. 1993), which is incorporated herein by reference.~~ Memory **100** includes a memory array **105** of multiple memory cells **110**. Row decoder **115** and column decoder **120** decode addresses provided on address lines **125** to access the addressed memory cells in memory array **105**. Command and control circuitry **130** controls the operation of memory **100** in response to control signals received on control lines **135** from a processor **140** or other memory controller during read, write, refresh, and erase operations. Command and control circuitry **130** includes a refresh circuit for periodically refreshing the data stored on the memory cells **110**. Voltage control **150** provides appropriate voltages to the memory cells during read, write, refresh, and erase operations. Memory **100**, as illustrated in Figure **1**, has been simplified for the purpose of illustrating the present invention and is not intended to be a complete description. Only the substantial differences between DEAPROM memory **100** and conventional DRAM and flash EEPROM memories are discussed below.

The paragraph beginning at page 12, line 11 is amended as follows:

The Fowler-Nordheim tunneling current density in gate insulator **225**~~, which~~ is illustrated approximately by Equation **3** below~~, is described in a textbook by S.M. Sze, "Physics of Semiconductor Devices," John Wiley & Sons, New York (1969), p. 496~~.

$$J=AE^2e^{\left(-\frac{B}{E}\right)} \qquad (3)$$

In Equation **3**, J is the current density in units of amperes/cm^2, E is the electric field in gate insulator **225** in units of volts/cm and A and B are constants, which are particular to the material of gate insulator **225**, that depend on the effective electron mass in the gate insulator **225** material and on the barrier energy Φ_{GI}. The constants A and B scale with the barrier energy Φ_{GI}, as illustrated approximately by Equations **4** and **5**~~, which are disclosed in S.R. Pollack et al., "Electron Transport Through Insulating Thin Films," Applied Solid State Science, Vol. 1, Academic Press, New York, (1969), p. 354~~.

$$A\alpha\left(\frac{1}{\Phi_{GI}}\right) \qquad (4)$$

$$B\alpha(\Phi_{GI})^{\frac{3}{2}} \qquad (5)$$

For a conventional floating gate FET having a 3.3 eV barrier energy at the interface between the polysilicon floating gate and the SiO_2 gate insulator, A = 5.5 x 10^{-16} amperes/Volt^2 and B = 7.07 x 10^7 Volts/cm~~, as disclosed in D.A. Baglee, "Characteristics and Reliability of 100 Å Oxides," Proc. 22nd Reliability Symposium, (1984), p. 152~~. One aspect of the present invention includes selecting a smaller barrier energy Φ_{GI} such as, by way of example, but not by way of limitation, $\Phi_{GI} \approx 1.08$ eV. The constants A and B for $\Phi_{GI} \approx 1.08$ eV can be extrapolated from the constants A and B for the 3.3 eV polysilicon-SiO_2 barrier energy using Equations **4** and **5**. The barrier energy $\Phi_{GI} \approx 1.08$ eV yields the resulting constants A = 1.76 x 10^{-15} amperes/Volt^2 and B = 1.24 x 10^7 Volts/cm.

The paragraph beginning at page 20, line 10 is amended as follows:

In one embodiment, a composition v of a polycrystalline $Ga_{1-v}Al_vN$ floating gate **215** is selected approximately between $0 < v < 1$ to obtain a desired barrier energy, as described below. The GaAlN floating gate **215** provides a lower electron affinity than polysilicon. The GaAlN floating gate **215** electron affinity can be approximately between 0.6 eV $< \chi_{215} <$ 2.7 eV as the

GaAlN composition variable ν is decreased from 1 to 0. ~~See V. M. Bermudez et al. "The Growth and Properties of Al and AlN films on GaN" J. Appl. Physics, Vol. 79, No. 1, pp. 110-119 (1996).~~ As a result, the GaAlN floating gate **215** provides a smaller resulting barrier energy Φ_{GI} than a polysilicon gate material having an electron affinity $\chi_{215} \approx 4.2$ eV. For example, using a SiO_2 gate insulator **225**, a barrier energy approximately between $-0.3 \text{ eV} < \Phi_{GI} < 1.8 \text{ eV}$ is obtained using an GaAlN floating gate **215** as the GaAlN composition ν varies between $\nu \approx 1$ (i.e., approximately AlN) and $\nu \approx 0$ (i.e., approximately GaN). By contrast, a conventional polysilicon floating gate material provides a barrier energy $\Phi_{GI} \approx 3.3$ eV at an interface with an SiO_2 gate insulator **225**.

The paragraph beginning at page 21, line 4 is amended as follows:

In one embodiment floating gate **215** is formed of a polycrystalline, microcrystalline, or nanocrystalline, GaN thin film that is CVD deposited on a thin (e.g., 500 Å thick) AlN buffer layer, such as by metal organic chemical vapor deposition (MOCVD), which advantageously yields improved crystal quality and reduced microscopic fluctuation of crystallite orientation. ~~See e.g., V. M. Bermudez et al. "The Growth and Properties of Al and AlN films on GaN" J. Appl. Physics, Vol. 79, No. 1, pp. 110-119 (1996). See also I. Akasaki et al. "Effects of AlN Buffer Layer on Crystallographic Structure and On Electrical and Optical Properties of GaN and $Ga_{1-x}Al_xN$ Films Grown on Sapphire Substrate by MOVPE," J. Of Crystal Growth, Vol. 98, pp. 209-19, North Holland, Amsterdam (1989).~~